

REMARKS

In the Parent Application, claims 1-7, 9-16, and 18-20 were pending and all were rejected under 35 U.S.C. § 102 in the Final Office Action mailed July 12, 2004. The rejection is traversed. A Request for Continued Examination (RCE) under 37 CFR 1.114 is being submitted together with this Preliminary Amendment in which claims 1, 4, 6, 10, 13, 15, and 19 are being amended; claims 2, 7, 9, 11, 16, and 18 are being canceled; and claims 21-26 are being added. In view of the above amendments and following remarks, reconsideration and allowance of the application is respectfully requested.

REJECTIONS UNDER 35 U.S.C. § 102(e) – Palanca

In paragraphs 5 and 6, claims 1-7, 9-16, and 18-20 were rejected under 35 U.S.C. § 102 (e) as being taught by U.S. Patent number 6,216,215 to Palanca et al. (“Palanca”). The rejection is traversed. Palanca failed to teach every element of the claimed invention.

For example, claim 1 is patentably distinguished from Palanca for at least the following reason. In general, in claim 1, the early-retirement criteria for retiring a first instruction is met when *processing a second instruction* in the various processing stages *causes* that continued processing of the first instruction does not change an architectural state of the system processing the first instruction, and, at the time of termination, the first instruction has completed its function without completing its full pipeline. The second instruction is different from the first instruction.

In contrast, the senior load instruction in Palanca does not update the architectural register state (col. 7, lines 12-13) and is a special type of load that can be retired before the data transfer is completed (col. 7, lines 1-3). Further, “[b]ecause it [the senior load instruction] does not ultimately change the architectural register state,

a senior load instruction can be retired before executing” (col. 7, lines 15-18). As can be seen, in Palanca, the senior load instruction by itself does not change the architectural state, but the fact that the architectural state does not change is not caused by processing a second instruction different from the senior load instruction as in the claimed invention. Therefore, claim 1 is patentably distinguished from Palanca and patentable.

Claims 3-6 depend directly or indirectly from claim 1 and are therefore patentable for at least the same reasons as claim 1. Claims 3-6 are also patentable for their additional limitations.

Claim 10 recites limitations corresponding to claim 1, and is therefore patentable for at least the same reasons as claim 1. Claims 12-15 depend directly or indirectly from claim 10 and are therefore patentable for at least the same reasons as claim 1. Claims 12-15 are also patentable for their additional limitations.

Claim 19 recites limitations corresponding to claim 1, and is therefore patentable for at least the same reasons as claim 1.

ADDED CLAIMS

Claims 21-26 are being added. Claims 21-23 depend directly or indirectly from claim 1 and are therefore patentable for at least the same reasons as claim 1. Claims 21-23 are also patentable for their additional limitations. For example, the limitations regarding “processing the second instructions comprises executing a branch condition of a branch instruction,” “terminating the first instruction includes discarding execution of a branch of the branch instruction,” and “processing the second instruction comprises loading a register with a value that the register already contains,” are not taught, suggested, or made obvious by Palanca.

Added independent claim 24 is patentable for at least the limitation that “wherein the early-retirement criteria is met when the instruction is identified as performing a logical OR of a register with the same register, writing a value 0 from a register into the same register, or writing a value to a register hardwired to a predetermined value,” which is not taught, suggested, or made obvious by Palanca.

Claim 25 depend from claim 24 and is patentable for at least the same reason as claim 24. Claim 25 is also patentable for its own limitation that is not taught, suggested or made obvious by Palanca, including, for example “one or a combination of the following steps to determine whether the early-retirement criteria is met: evaluating an op-code of the instruction; and evaluating a register target of the instruction.”

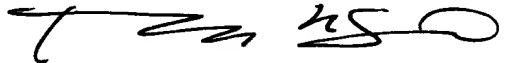
Independent claim 26 is patentable for at least the limitations that the method relates to retiring early a NO-OP instruction; evaluating an op-code of the instruction to determine whether the instruction is the NO-OP instruction; using a tag to indicate that the NO-OP instruction has met the early-retirement criteria; which are not taught, suggested, or made obvious by Palanca.

SUMMARY

In conclusion, it is respectfully submitted that pending claims 1, 3-6, 10, 12-15, and 19, and added claims 21-26 clearly present subject matter that is patentable over the prior art of record, and therefore withdrawal of the rejections and reconsideration of the claims are respectfully requested.

Respectfully submitted,

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